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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/759,557	01/12/2001	John Lee Barry	04148P013	9690

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DARBY & DARBY P.C.
P.O. BOX 5257
NEW YORK, NY 10150-5257

EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/759,557	BARRY ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *50-98* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *50-98* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 50-73, drawn to 50. (New) A method for testing a television, comprising: selecting a data pattern from a set of at least one pre-programmed data pattern, wherein each pre-programmed data pattern of the set of at least one pre-programmed data pattern includes a plurality of portions; creating the selected data pattern, wherein creating the selected data pattern includes: for each of the plurality of portions of the selected data pattern that is pre-programmed for algorithmic pattern generation, performing a pre-programmed algorithm to create the portion; and for each of the plurality of portions of the data patterns that is stored based on the pre-programming of the selected data pattern, retrieving the portion, classified in class 714, subclass 738.

II. Claims 74-82, drawn to generating a computer-readable algorithm that is configured to provide at least one portion of a plurality of portions of a data pattern through algorithmic pattern generation; and storing at least. one other portion of the plurality of portions in a look-up table, classified in class 714, subclass 759.

III. Claims 83-93, drawn to a pattern selection register that is arranged to store and provide a pattern select value indicating a selected data pattern

of a set of at least one pre-programmed data pattern, wherein each pre-programmed data pattern in the set of at least one pre- programmed data pattern includes a plurality of portions; a look-up table component that stores a portion in the plurality of portions of each of the pre-programmed data patterns in the set of at least one pre-programmed data pattern; and a state machine that is configured to enable the selected data pattern to be generated based on the pattern selection value, wherein state machine is configured to enable the selected data pattern to be generated by: controlling a retrieval of the portion of the selected data pattern from the look-up table; and based on the pre-programming, controlling a sequencing for algorithmic pattern generation of another portion of the selected data pattern, classified in class 714, subclass 734.

IV. Claim 94, drawn to a look-up table component that is configurable to sfore a portion of each of a plurality of data patterns; a state machine that is configurable to provide, if one of the plurality of data patterns is selected, a sequencing for algorithmic pattern generation of another portion of the selected data pattern; an output register that is configured to provide a regenerated selected data pattern based, in part, on the sequencing; and a built-in self test circuit that is configured to perform actions including during a configuration, determining and storing at least one checksum for determining at least one checksum for the regenerated selected data each of the plurality of data patterns; pattern; and comparing the at least one

checksum for the regenerated selected data pattern with the at least one stored checksum for the selected data pattern, classified in class 714, subclass 807.

V. Claims 95 and 96, drawn to a pattern selection register that is arranged to store and provide a pattern selection value indicating a selected data pattern of a plurality of component video data patterns, wherein each component video data pattern in the plurality of component video data patterns includes a plurality of portions; a pattern generation state machine that is arranged to control a sequencing of a regeneration of the selected data pattern by providing a plurality of clear and increment signals; a memory component that is arranged to provide a table output value based on the plurality of clear and increment signals and the pattern selection value, wherein the memory component includes: a line index table that stores values indicating a number of lines to transmit before switching to and from vertical blanking lines to active video lines; a header table that stores: a plurality of forty-bit data samples that each include a unique data word; and a sequence of data that includes a portion of a repeating vertical blanking data sequence for the vertical blanking lines, and further includes a repeat field that indicates a number of repetitions for the repeating vertical blanking sequence; a color table; a PLL pathological table; and an equalizer pathological table; a plurality of logic gates that are arranged to select one of two values associated with reading from the

equalizer pathological table based on a line count value and the pattern selection value; an output register that is arranged to regenerate the selected data pattern based, in part, on the table output value; a built-in self test circuit that is arranged to perform actions, including: during a configuration, determining and storing at least one checksum for each of the plurality of component video data patterns; determining at least one checksum for the regenerated selected data pattern; and comparing the at least one checksum for the regenerated selected data pattern with the at least one stored checksum for the selected data pattern; and a BIST result output pin that is configured to provide a BIST result signal that indicates a result of the comparison, classified in class 714, subclass 737.

VI. Claims 97 and 98, drawn to configuring a state machine with, for each of a plurality of component video data patterns, a sequencing for regenerating each of the component video data patterns; configuring a header table to store: a plurality of forty-bit data samples that each include a unique data word; and a sequence of data that includes a portion of a repeating vertical blanking data sequence for vertical blanking lines, and further includes a repeat field that indicates a number of repetitions for the repeating vertical blanking sequence; configuring a line index table to store values indicating a number of lines to transmit before switching to and from the vertical blanking lines to active video lines; configuring a color table, a PLL pathological table, and an equalizer pathological table

for algorithmic pattern generation of portions of each of the plurality of component video data patterns for the active video lines; determining and storing at least one checksum for each of the plurality of component video data patterns; selecting one of the plurality of component video patterns; providing a plurality of clear and increment signals based on the sequencing for regenerating the selected component video pattern; employing the header table, the color table, the PLL pathological table, the equalizer pathological table, and the line index table to regenerate the selected data pattern based, in part on the plurality of clear and increment signals; concurrently: displaying a video picture based on the regenerated selected test pattern; and providing regenerated selected test pattern to a built-in self test circuit; and employing the built-in self test circuit to: generate at least one BIST checksum from the regenerated selected data pattern; compare the at least one BIST checksum with the at least one stored checksum for the selected data pattern; and provide a result of the comparison to a BIST result output pin, classified in class 714, subclass 820.

The inventions are distinct, each from the other because of the following reasons:

Inventions Groups I, II and VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I has separate utility such as for a method for testing a television, comprising: selecting a

data pattern from a set of at least one pre-programmed data pattern, wherein each pre-programmed data pattern of the set of at least one pre-programmed data pattern includes a plurality of portions; creating the selected data pattern, wherein creating the selected data pattern includes: for each of the plurality of portions of the selected data pattern that is pre-programmed for algorithmic pattern generation, performing a pre-programmed algorithm to create the portion; and for each of the plurality of portions of the data patterns that is stored based on the pre-programming of the selected data pattern, retrieving the portion. In the instant case, invention Group II has separate utility such as for generating a computer-readable algorithm that is configured to provide at least one portion of a plurality of portions of a data pattern through algorithmic pattern generation; and storing at least. one other portion of the plurality of portions in a look-up table. In the instant case, invention Group VI has separate utility such as for configuring a state machine with, for each of a plurality of component video data patterns, a sequencing for regenerating each of the component video data patterns; configuring a header table to store: a plurality of forty-bit data samples that each include a unique data word; and a sequence of data that includes a portion of a repeating vertical blanking data sequence for vertical blanking lines, and further includes a repeat field that indicates a number of repetitions for the repeating vertical blanking sequence; configuring a line index table to store values indicating a number of lines to transmit before switching to and from the vertical blanking lines to active video lines; configuring a color table, a PLL pathological table, and an equalizer pathological table for algorithmic pattern generation of portions of each of the plurality of component video

data patterns for the active video lines; determining and storing at least one checksum for each of the plurality of component video data patterns; selecting one of the plurality of component video patterns; providing a plurality of clear and increment signals based on the sequencing for regenerating the selected component video pattern; employing the header table, the color table, the PLL pathological table, the equalizer pathological table, and the line index table to regenerate the selected data pattern based, in part on the plurality of clear and increment signals; concurrently: displaying a video picture based on the regenerated selected test pattern; and providing regenerated selected test pattern to a built-in self test circuit; and employing the built-in self test circuit to: generate at least one BIST checksum from the regenerated selected data pattern; compare the at least one BIST checksum with the at least one stored checksum for the selected data pattern; and provide a result of the comparison to a BIST result output pin. See MPEP § 806.05(d).

Inventions Groups III, IV and V are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group III has separate utility such as for a pattern selection register that is arranged to store and provide a pattern select value indicating a selected data pattern of a set of at least one pre-programmed data pattern, wherein each pre-programmed data pattern in the set of at least one pre- programmed data pattern includes a plurality of portions; a look-up table component that stores a portion in the plurality of portions of each of the pre-programmed data patterns in the set of at least one pre-programmed data pattern; and

a state machine that is configured to enable the selected data pattern to be generated based on the pattern selection value, wherein state machine is configured to enable the selected data pattern to be generated by: controlling a retrieval of the portion of the selected data pattern from the look-up table; and based on the pre-programming, controlling a sequencing for algorithmic pattern generation of another portion of the selected data pattern. In the instant case, invention Group IV has separate utility such as for a look-up table component that is configurable to sfore a portion of each of a plurality of data patterns; a state machine that is configurable to provide, if one of the plurality of data patterns is selected, a sequencing for algorithmic pattern generation of another portion of the selected data pattern; an output register that is configured to provide a regenerated selected data pattern based, in part, on the sequencing; and a built-in self test circuit that is configured to perform actions including during a configuration, determining and storing at least one checksum for determining at least one checksum for the regenerated selected data each of the plurality of data patterns; pattern; and comparing the at least one checksum for the regenerated selected data pattern with the at least one stored checksum for the selected data pattern. In the instant case, invention Group V has separate utility such as for a pattern selection register that is arranged to store and provide a pattern selection value indicating a selected data pattern of a plurality of component video data patterns, wherein each component video data pattern in the plurality of component video data patterns includes a plurality of portions; a pattern generation state machine that is arranged to control a sequencing of a regeneration of the selected data pattern by providing a plurality of

clear and increment signals; a memory component that is arranged to provide a table output value based on the plurality of clear and increment signals and the pattern selection value, wherein the memory component includes: a line index table that stores values indicating a number of lines to transmit before switching to and from vertical blanking lines to active video lines; a header table that stores: a plurality of forty-bit data samples that each include a unique data word; and a sequence of data that includes a portion of a repeating vertical blanking data sequence for the vertical blanking lines, and further includes a repeat field that indicates a number of repetitions for the repeating vertical blanking sequence; a color table; a PLL pathological table; and an equalizer pathological table; a plurality of logic gates that are arranged to select one of two values associated with reading from the equalizer pathological table based on a line count value and the pattern selection value; an output register that is arranged to regenerate the selected data pattern based, in part, on the table output value; a built-in self test circuit that is arranged to perform actions, including: during a configuration, determining and storing at least one checksum for each of the plurality of component video data patterns; determining at least one checksum for the regenerated selected data pattern; and comparing the at least one checksum for the regenerated selected data pattern with the at least one stored checksum for the selected data pattern; and a BIST result output pin that is configured to provide a BIST result signal that indicates a result of the comparison. See MPEP § 806.05(d).

Inventions Groups I, V & VI and Groups III, IV & V are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1)

the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the process, Groups I, V & VI, can be carried out in software.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I, II, III, IV, V & VI is mutually exclusive, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

A telephone call was made to Mathew Gaffney on 11/2/2004 to request an oral election to the above restriction requirement, but did not result in an election being made.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim

remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133